PROCESS FOR FORMING POLYCRYSTALLINE SILICON LAYER BY LASER CRYSTALLIZATION

FIELD OF THE INVENTION

[0001] The present invention relates to a process for forming a polycrystalline silicon layer, and more particularly to a process for forming a polycrystalline silicon layer with large crystal grain size and high uniformity by laser crystallization.

BACKGROUND OF THE INVENTION

[0002] Polycrystalline silicon thin film transistors are commonly used as basic electronic devices for controlling pixels of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). In addition, the polycrystalline silicon thin film transistors are also used as basic electronic devices required by the peripheral driving circuits and/or control circuits in these displays.

[0003] During production of the polycrystalline silicon thin film transistors (TFTs), the crystallization procedure for forming a polycrystalline silicon layer is critical. The electrical properties and uniformity of the polycrystalline silicon thin film transistors are primarily determined by this procedure.

[0004] A conventional process for forming a polycrystalline silicon layer using a crystallization method is illustrated with reference to Figs. 1(a) and 1(b). Firstly, an amorphous silicon layer 104 is formed on a glass or plastic substrate 100. Then, the amorphous silicon layer 104 is irradiated with an excimer laser to be molten. The molten amorphous silicon layer is cooled and recrystallized into a polycrystalline silicon layer 105.

[0005] Referring to Fig. 2, the relationship between the energy density of an excimer laser irradiating on the amorphous silicon layer and the electrical property such as the electron mobility of the resulting recrystallized polycrystalline silicon layer is shown. As shown, the energy density effective for forming a polycrystalline silicon layer with good electrical property is confined to a narrow range. An excessive energy density may result in microcrystalline silicon rather than polycrystalline silicon. The electrical property of microcrystalline silicon is different from that of the polycrystalline silicon. For example, its electron mobility is not as high as required in some applications. On the other hand, an insufficient energy density substantially fails to effectively melt the amorphous silicon for subsequent recrystallization.

[0006] Furthermore, due to the variability of the excimer laser, the grain size of the recrystallized polycrystalline silicon layer 105 may be too small and non-uniform, and thus the electron property of the thin film transistor product varies significantly.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide a process for forming a polycrystalline silicon layer consisting of relatively uniform and large crystal grains.

[0008] It is another object of the present invention to provide a process for forming a polycrystalline silicon layer with a less critical energy-density range of an pulse laser for the crystallization of the polycrystalline silicon layer.

[0009] In accordance with a first aspect of the present invention, there is provided a process for forming a polycrystalline silicon layer. Firstly, at least one seed is formed on a substrate. Then, an amorphous silicon layer is formed on the substrate and overlies the seed. Then, the amorphous silicon layer is

irradiated with a laser to melt the amorphous silicon layer. Afterward, the molten amorphous silicon layer is recrystallized to form a polycrystalline silicon layer.

[0010] In one embodiment, the step of forming the at least one seed on the substrate comprises sub-steps of forming an intermediate covering layer on the substrate, patterning the intermediate covering layer to define the intermediate covering layer as a specified pattern, forming an amorphous silicon spacer beside the specified pattern, and removing the specified pattern with the spacer remained.

[0011] For example, the substrate is a glass substrate or a plastic substrate, the laser is an excimer laser, and the intermediate covering layer is made of silicon nitride or metal.

[0012] In accordance with a second aspect of the present invention, there is provided a process for forming a polycrystalline silicon layer. Firstly, a first region and a second region on a substrate are defined. Then, at least one seed on the first region of the substrate is formed. Then, an amorphous silicon layer is formed on the first and the second regions of the substrate. Then, the amorphous silicon layer is irradiated with a laser to melt the amorphous silicon layer. Afterward, the molten amorphous silicon layer is recrystallized on the first region to form a polycrystalline silicon layer.

[0013] If necessary, the process can further comprise a step of recrystallizing the molten amorphous silicon layer on the second region to form a microcrystalline silicon layer.

[0014] In accordance with a third aspect of the present invention, there is provided a process for fabricating a polycrystalline silicon layer. Firstly, a substrate is provided. Then, an intermediate covering layer is formed on the

substrate. Then, the intermediate covering layer is patterned to define the intermediate covering layer as a specified pattern. Then, an amorphous silicon spacer is formed beside the specified pattern. Then, the specified pattern with the spacer remained is removed to form at least one seed the substrate. An amorphous silicon layer is then formed on the substrate and overlies the seed. Then, the amorphous silicon layer is irradiated with a laser to melt the amorphous silicon layer. Afterward, the molten amorphous silicon layer is recrystallized to form a polycrystalline silicon layer.

[0015] Accordingly, the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figs. 1(a) and 1(b) are schematic cross-sectional diagrams illustrating a conventional process for forming a polycrystalline silicon layer by using a crystallization method;

[0017] Fig. 2 is a plot showing the electron mobility change and phase change with the energy density of an excimer laser irradiating on the amorphous silicon layer according to prior art;

[0018] Figs. 3(a) to 3(i) are schematic cross-sectional diagrams illustrating a process for forming a polycrystalline silicon layer of a thin film transistor according to an embodiment of the present invention;

[0019] Fig. 4(a) is a top view of a polycrystalline silicon layer formed according to the process of the present invention;

[0020] Fig. 4(b) is a top view of the polycrystalline silicon layer of Fig. 4(a) formed thin film transistors;

[0021] Fig. 5 is a plot showing the electron mobility change and phase change with the energy density of a pulsed laser irradiating on the amorphous silicon layer according to the present invention; and

[0022] Fig. 6 is a schematic diagram illustrating the simultaneous formation of polycrystalline silicon and microcrystalline silicon regions to obtain two kinds of thin film transistors.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0023] A process for forming a polycrystalline silicon layer of a thin film transistor is illustrated with reference to Figs. 3(a) to 3(i).

[0024] In Fig. 3(a), an intermediate covering layer 204, for example made of silicon nitride (SiNx) or metal, is formed on a substrate 200 such as a glass or a plastic substrate.

[0025] Then, as shown in Fig. 3(b), a photoresist 206 is formed on the intermediate covering layer 204 and properly patterned to cover selected regions of the intermediate covering layer 204. The intermediate covering layer 204 is then etched with the photoresist 206 serving as a mask. After the etching procedure is completed and the photoresist 206 is removed, a specified pattern of the intermediate covering layer 204 is obtained, as can be seen in Fig. 3(c).

[0026] In Fig. 3(d), an amorphous silicon layer 208 is then formed on the resulting structure of Fig. 3(c). An anisotropic etching procedure is subsequently performed on the amorphous silicon layer 208, thereby forming amorphous spacers 210 beside the specified pattern of the intermediate covering layer 204, as can be seen in Fig. 3(e).

[0027] Then, as shown in Fig. 3(f), the specified pattern of the intermediate covering layer 204 is removed, but the amorphous spacers 210

remain on the substrate 200. The remaining amorphous spacers 210 are used as seeds for the following crystallization procedure.

[0028] In Fig. 3(g), additional amorphous silicon layer 212 is formed on the substrate 200 and overlies the seeds 210. Then, as shown in Fig. 3(h), the amorphous silicon layer 212 is irradiated with a pulse laser (for example an excimer laser) to melt the amorphous silicon layer 212. By controlling energy density of the pulse laser, the amorphous silicon layer 212 can be fully melted. Meanwhile, the seeds 210 remaining on the substrate 200 will not be fully molten. In such manner, when the molten amorphous silicon layer 212 is cooled, the seeds 210 will promote formation of relatively uniform and large crystal grains along both sides of the seeds (in the arrow directions). Thus, the molten amorphous silicon layer 212 is recrystallized to form a polycrystalline silicon layer 212a as shown in Fig. 3(i), and grain boundaries 214 are formed in the polycrystalline silicon layer 212a.

[0029] The polycrystalline silicon layer formed according to the process of the present invention is illustrated in Fig. 4(a). In Fig. 4(a), the regions between two dotted lines indicate the location of the seeds 210, while the solid lines indicate the grain boundaries 214, respectively. Afterwards, thin film transistors are formed by any of suitable manufacturing processes, which are not intended to be described redundantly herein. In Fig. 4(b), the hatched portions indicate the location of the thin film transistors, and the source electrodes S, the gate electrodes G, the drain electrodes D and thus channels of the thin film transistors are shown.

[0030] As previously described, the energy density of the pulse laser (for example an excimer laser) effective for forming a polycrystalline silicon layer with good electrical property is confined to a narrow range. The improper

energy density is likely to result in the formation of microcrystalline silicon instead of desired polycrystalline silicon or result in non-uniform grain size of the recrystallized polycrystalline silicon layer. According to the present invention, seeds are additionally provided between the substrate and the amorphous silicon layer prior to the formation of the amorphous silicon layer. Accordingly, when a certain energy density of excimer laser required for melting the amorphous silicon layer in the prior art, or even if a little more intense excimer, is applied to the amorphous silicon layer of the present invention for the same period of time, the seeds are protected from being molten away. In other words, the energy-density range of an excimer laser suitable for melting and recrystallizing the amorphous silicon layer into the polysillicon layer can be broadened. Referring to Fig. 5, the relationship between the energy density of a pulse laser irradiating on the amorphous silicon layer and the electrical property such as the electron mobility of the resulting recrystallized polycrystalline silicon layer is shown. As shown, the energy density effective for forming a polycrystalline silicon layer with good electrical property is broadened. After the amorphous silicon layer is fully melted and then cooled, the molten amorphous silicon layer is recrystallized starting from sides of the seeds so as to form a polycrystalline silicon layer with relatively uniform and large crystal grains.

[0031] In practice, while some thin film transistors require gate channels formed of polycrystalline silicon layers, others require gate channels made of microcrystalline silicon layers. Sometimes, two types of thin film transistors respectively with these two gate channels are required to be formed on the same glass substrate. Conventionally, these two types of thin film transistors have to be separately manufactured. Such conventional process is complicated and has

unsatisfactory reliability. According to the present invention, these two types of transistors can be formed on the glass substrate simultaneously so as to reduce fabrication cost. Referring to Fig. 6, it is assumed that a first region 220 and a second region 240 on a glass substrate are to be formed thereon two types of transistors with polycrystalline silicon and microcrystalline silicon gate channels, respectively. Seeds are first formed on the first region 220 in a manner as described in the above embodiment, but no seeds are formed on the second region 240. Then, an amorphous silicon layer (not shown) is formed on and overlies the first region 220 and the second region 240. The amorphous silicon layer is irradiated with a sufficient intensity of pulse laser to be completely molten. Due to the presence of the remaining seeds after the melting procedure in the first region 220, a polycrystalline silicon layer with relatively uniform and large crystal grains is formed on the first region 220 in the subsequent cooling procedure. Meanwhile, a microcrystalline silicon layer is formed in the second region 240.

[0032] From the above description, it is understood that the process for forming a polycrystalline silicon layer by burying seeds under the amorphous silicon layer in advance can make the condition of the applied pulse laser less critical so as to easily obtain a polycrystalline silicon layer with relatively uniform and large crystal grains and thus thin film transistor products with stable electron properties.

[0033] While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended

claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.